ACSL_Signal_Entity VTB Model

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Model name: ACSL_Signal_Entity
DLL name: ACSL_Signal_Entity.vtm
Version number: 1.0
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Pictorial Representation of Model

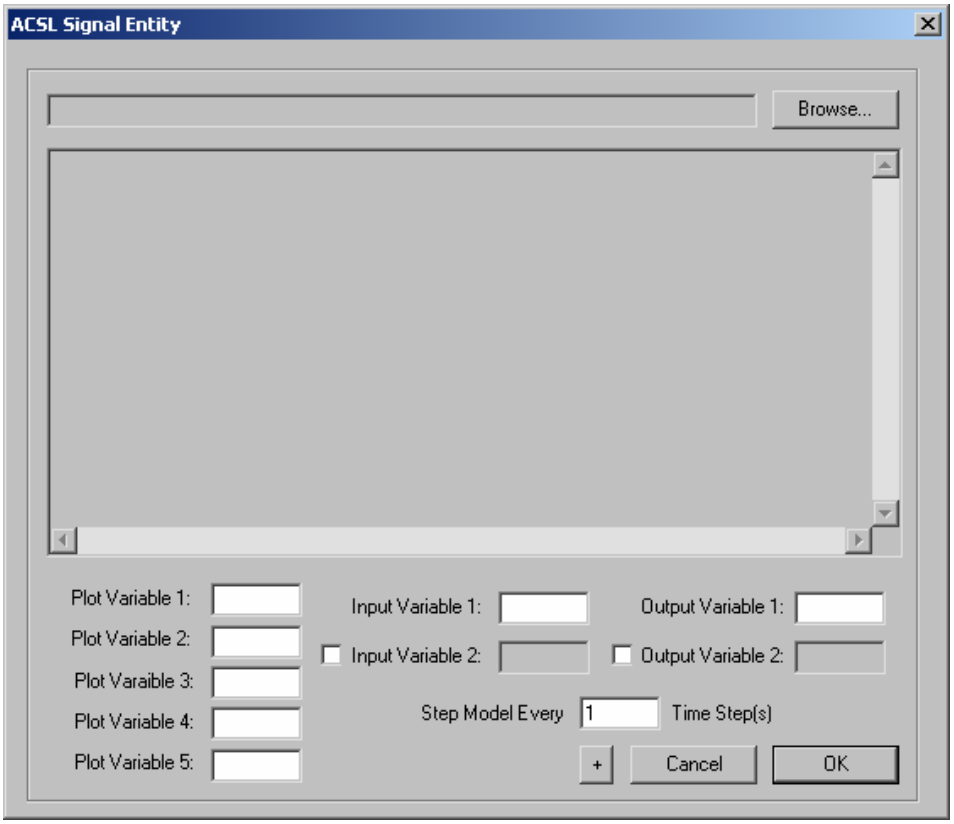

Figure 1 - ACSL Signal Entity properties dialog

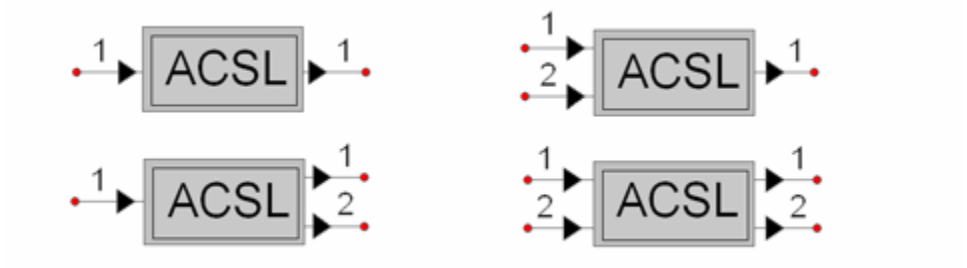

Figure 2 - ACSL Signal Entity icons

Brief Description of Model

This model wraps a model made by ACSL. The model allows for various numbers of inputs and outputs to the circuit. The connection is a signal coupling done by modified nodal analysis.

Model Validity Range and Limitations

There can only be one ACSL model in any schematic. This is a limitation of the ACSL API (Application Programmers Interface) provided by the makers of ACSL.

List of Model Pins with Connectivity Information

Pin Designation	Description
Input 1	The voltage at this pin will be input to a variable of the ACSL model. The variable will be determined by the corresponding parameter value (see parameter descriptions).
Input 2	The voltage at this pin will be input to a variable of the ACSL model. The variable will be determined by the corresponding parameter value (see parameter descriptions).
Output 1	The internal ACSL value of a variable will be shown as a magnitude at this pin. It will act as an ideal voltage source. The variable is determined by its corresponding parameter value (see parameter descriptions).
Output 2	The internal ACSL value of a variable will be shown as a magnitude at this pin. It will act as an ideal voltage source. The variable is determined by its corresponding parameter value (see parameter descriptions).

List of Parameters and Output Variables

This is a complete list of all parameters of the model. All models use SI units.

Parameter Name	Description	Default Value	Units
ACSL model file path	This is the path to the ACSL model to use.	Empty	N/A
Input variable 1	The exact name of the ACSL variable that will receive the input value from input pin 1.	Empty	Dependent on the coupling type selected
Output variable 1	The exact name of the ACSL variable whose value will be output on output pin 1.	Empty	Dependent on the coupling type selected
Coupling Type	The type of ideal source that the model should be in the simulation.	VCCS	N/A
ACSL plot variable 1	Name of internal ACSL variable that will be viewable.	Empty	N/A
ACSL plot variable 2	Name of internal ACSL variable that will be viewable.	Empty	N/A

ACSL plot variable 3	Name of internal ACSL variable that will be viewable.	Empty	N/A
ACSL plot variable 4	Name of internal ACSL variable that will be viewable.	Empty	N/A
ACSL plot variable 5	Name of internal ACSL variable that will be viewable.	Empty	N/A
Number of steps in VTB before stepping the ACSL model	This parameter allows the ACSL model to be stepped at some multiple of the step used in VTB	1 step	N/A
ACSL stop variable name	The name of the ACSL variable that is used to determine the stop condition for the ACSL model	TSTOP	N/A

This is a list of output variables.

Variable Name	Description	Units
Output 1	The output at output pin 1.	N/A
Output 2	The output at output pin 2	N/A
ACSL variable 1	An internal ACSL variable that can be plotted.	N/A
ACSL variable 2	An internal ACSL variable that can be plotted.	N/A
ACSL variable 3	An internal ACSL variable that can be plotted.	N/A
ACSL variable 4	An internal ACSL variable that can be plotted.	N/A
ACSL variable 5	An internal ACSL variable that can be plotted.	N/A

Assumptions in Model Derivation

The model is coupled to the containing VTB system as an ideal controlled voltage source.

Mathematical Description of Model

N/A

Example of Model Use

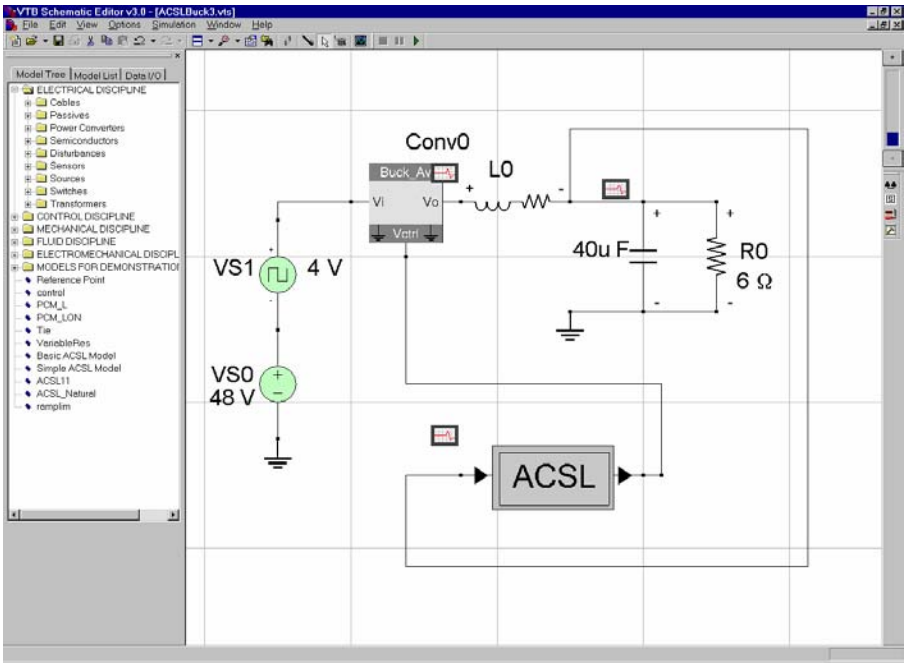

Figure 3 – Circuit for model verification

The figure above shows the VTB schematic representing a closed-loop buck-type switching power converter. The power cell is described using VTB native models while the control system is described using ACSL format. The input to the ACSL signal flow model is the feedback voltage and the output is the converter duty-cycle calculated according to the feedback compensation law.

Model Validation

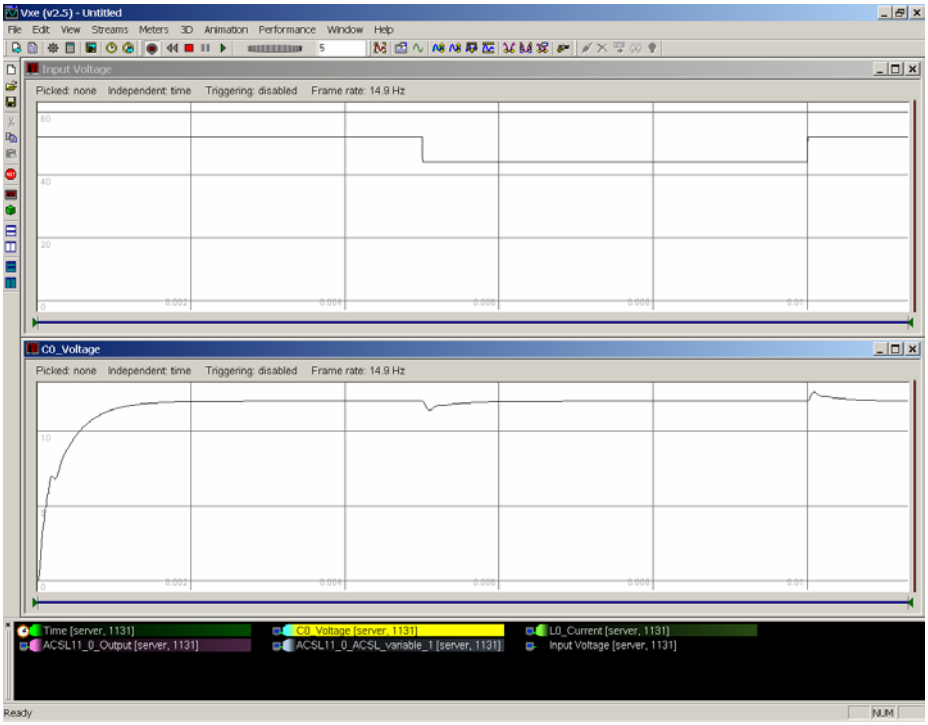

Figure 4 – Test circuit results

To check the performance of the controller a disturbance is introduced into the source. The simulation results are shown. The upper trace presents the reference voltage while the lower trace presents the output voltage. The control behaves as expected, rejecting the input voltage variation after a short transient, confirming that the simulation link was effective.

References

W. McKay, A. Monti, E. Santi and R. Dougal, *A Co-Simulation Approach for ACSL-Based Models*, Huntsville Simulation Conference, Huntsville, AL, October 3-4, 2001.