***Project:*** MVDC Fault Management

***Project Completion:*** 2017

***Output:*** A technical report [1] and multiple conference papers pertaining to MVDC fault management were written throughout this project [2 - 10].

***Outcome:***

1. Demonstrated current limiting capabilities of current limiting Modular Multilevel Converters (MMC) at the megawatt level in a Medium Voltage Direct Current (MVDC) testbed.
2. Developed a fault clearance sequence for MVDC shipboard power systems (SPS) with current limiting converters and fast disconnect switches.
3. Developed and demonstrated a centralized fault location algorithm for MVDC SPS in a controller hardware-in-the-loop environment.
4. Demonstrated the fault clearance sequence at the megawatt level utilizing an MVDC testbed
5. Tested and provided in depth analysis of arc faults anticipated in fault current limited MVDC systems.
6. Developed a graph traversal-based method for automating system-wide programming of differential fault protection and generation of fault isolation steps in MVDC shipboard power systems (SPS).

***Project Motivation:*** The increasing demand for power and energy and a vision for an all-electric ship has created an interest in research on Medium Voltage DC (MVDC) Power systems. MVDC system have advantages over conventional AC systems when comparing the power density, flexibility, reliability and efficiency of power distribution. Although DC distribution systems provide these great advantages enthusiasm for adopting DC technologies suffers from widespread concern over the means to protect DC distribution systems against short-circuit faults, ground faults, and open-circuit ("series") faults, especially at medium voltage levels. Fault management in MVDC shipboard power systems (SPS) is an important aspect and requires a rapid, and highly-coordinated response from system components.

The work conducted here mainly focused on fault management in breaker-less MVDC architectures with fault current limiting converters. Clearing of short circuits and fast system restoration is an important aspect on MVDC shipboard power systems (SPS) with current limiting modular multilevel converters (MMC) and fast disconnect switches. With this in mind, the fault clearance sequence (as shown in Figure 1) was developed which consist of 4 steps:

1. Fault location detection- When a fault occurs in the system, the MMCs switch into current limiting mode and the CFL detects and locates the fault in about 800 μs.
2. 2. After the fault is located, the system is completely de-energized by bringing the system voltage and current to zero.
3. 3. Once the system is completely de-energized, the fast disconnect switches associated with the corresponding fault location are opened thereby isolating the fault.
4. 4. After the faulted section is isolated from the system, the system is reenergized to resume normal operation.

The rapid power transfer and fault current limiting performance of Modular Multilevel Converters (MMCs) under normal and fault scenarios were tested in simulation, controller hardware-in-loop (CHIL), and power hardware-in-loop (PHIL) environments [2 - 4] and [7 - 10].

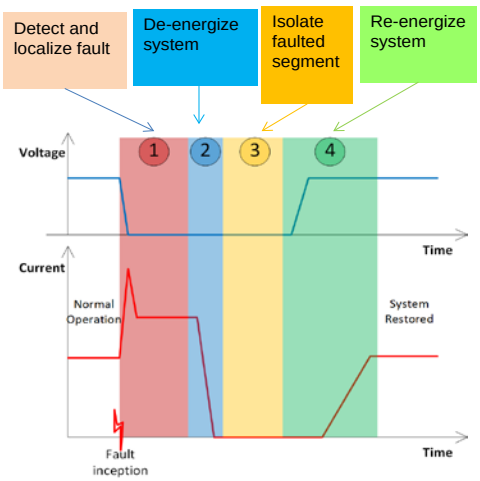


*Figure 1: Fault Clearing Sequence*

***Project Extent:*** This project involved multiple researchers from several ESRDC institutions and has been documented in a technical report [1], and multiple conference papers [2]-[10].

***Technical Point of Contact:*** Harsha Ravindra (ravindra@caps.fsu.edu)

***References:***


[1]. Technical Report submitted to Office of Naval Research (ONR), “Fault current limiting methods”, October 2013.

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[3]. K. Sun, D. Soto, M. Steurer and M. O. Faruque, "Experimental verification of limiting fault currents in MVDC systems by using modular multilevel converters," 2015 IEEE Electric Ship Technologies Symposium (ESTS), Alexandria, VA, 2015, pp. 27-33.

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[6]. D. Soto, R. Soman, M. Sloderbeck, M. Steurer, and P. Zeller, “High-Speed camera imaging of arc faults anticipated in fault current limited MVDC systems,” 2016 American Society of Naval Engineers (AMTS) Conference, Philadelphia, PA, USA, 2016.

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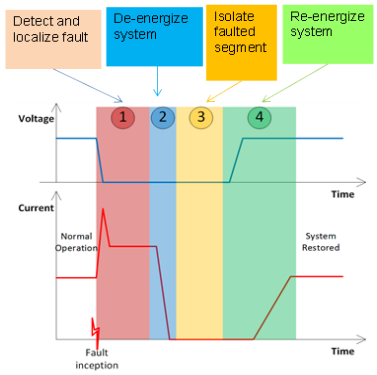
[10]. C. Diendorfer et al., "Graph traversal-based automation of fault detection, location, and recovery on MVDC shipboard power systems," 2017 IEEE Second International Conference on DC Microgrids (ICDCM), Nuremburg, 2017, pp. 119-124.

# MVDC Fault Management

## Motivation

- Increasing demand for power and energy and a vision for an all-electric ship created an interest in research on Medium Voltage DC (MVDC) Power systems.
- MVDC system have advantages over conventional AC systems when comparing the power density, flexibility, reliability and efficiency of power distribution.
- DC technologies suffer from widespread concern over the means to protect DC distribution systems against short-circuit faults, ground faults, and open-circuit ("series") faults, especially at medium voltage levels
- Fault management in MVDC shipboard power systems (SPS) is an important aspect and requires a rapid, and highly-coordinated response from system components




## Approach

- **Centralized Fault Location Algorithm**
  - Developed and tested in a simulation only environemt
  - Developed and tested in a CHIL environment utilizing commecially available hardware
- **Current limiting and Arc faults testing with MMCs**
  - Tested in a CHIL environment to derisk the system
  - Tested in an MVDC testbed using the real hardware and utilized a high speed camera to better study the arc fault behaviors
- **Fault clearance sequence**
  - Developed and tested in a simulation only environment
  - Developed and tested in a CHIL enviroment
  - Developed and tested in an MVDC testbed at MW power levels
- **Traversal-based method for fault protection and isolation steps**
  - Developed and tested in a simulation and CHIL environment

## Outcomes

- Demonstrated current limiting capabilities of current limiting Modular Multilevel Converters (MMC) at the megawatt level in a MVDC testbed.
- Developed a fault clearance sequence for MVDC shipboard power systems (SPS) with current limiting converters and fast disconnect switches which was achieved in less than 25 ms.
- Developed and demonstrated a centralized fault location algorithm for MVDC SPS in a controller hardware-in-the-loop environment which successfully detected fault locations in less than 1 ms.
- Tested and provided in depth analysis of arc faults anticipated in fault current limited MVDC systems.
- Developed a graph traversal-based method for automating system-wide programming of differential fault protection and generation of fault isolation steps in MVDC SPS.